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APPLICATION FOR U.S. LETTERS PATENT

Title:

REMOVABLE PROGRAMMABLE CONDUCTOR MEMORY CARD AND ASSOCIATED READ/WRITE DEVICE AND METHOD OF OPERATION

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TITLE OF INVENTION

REMOVABLE PROGRAMMABLE CONDUCTOR MEMORY CARD AND ASSOCIATED READ/WRITE DEVICE AND METHOD OF OPERATION

FIELD OF THE INVENTION

[0001] The invention relates to non-volatile memory devices using programmable conductor random access memory (PCRAM) arrays.

BACKGROUND OF THE INVENTION

[0002] There is a trend toward use of removable non-volatile memory devices such as flash memory devices in digital cameras and other devices which benefit from removable non-volatile memory. Conventional non-volatile memory devices typically have limited density, high manufacturing cost, and high power consumption. A lower cost alternative to flash and other conventional removable non-volatile memory devices is desirable.

BRIEF SUMMARY OF THE INVENTION

[0003] In one aspect, the invention provides a programmable conductor random access memory (PCRAM) apparatus and method of operation which uses a removable PCRAM memory card comprising a programmable conductor material, e.g. a chalcogenide glass, layer containing a plurality of data storing memory elements. A housing into which the card can be inserted contains a read/write assembly containing conductive elements which define and/or align with previously defined memory elements of the card. The conductive elements

are in removable contact with the memory cells of the card and are used to read and write data from and to the memory elements of the card.

[0004] The invention also provides a removable card formed of a programmable conductor material, e.g. chalcogenide glass, which can be used with a read/write assembly to define and program memory elements within the programmable conductor material.

[0005] The invention also provides a removable memory card formed of a programmable conductor material, e.g. a chalcogenide glass, which has a plurality of memory elements defined therein and which can be used for temporary or permanent storage and in which both temporary and permanent storage cells can simultaneously coexist on the same memory card.

BRIEF DESCRIPTION OF THE DRAWING

[0006] The foregoing and other features and advantages of the invention will become more apparent from the detailed description of the exemplary embodiments of the invention given below in connection with the accompanying drawings in which:

[0007] Figure 1 is a schematic diagram depicting an proposed PCRAM device;

[0008] Figure 2A and Figure 2B depict PCRAM memory cards which are employed in the invention;

[0009] Figure 3A and 3B respectively illustrate a perspective view and cutaway side view of a card reading and writing device which may be used with the Figure 2 and Figure 2B memory card;

[00010] Figure 4 illustrates in perspective view a portion of a read/write assembly which may be employed as part of the mechanism illustrated in Figure 3B;

[00011] Figure 5 represents a portion of the read/write structure illustrated in Figure 3B;

[00012] Figure 6 illustrates in schematic form the electrical interconnection of the Figure 5 structure with the Figure 2A, 2B memory card;

[00013] Figure 7 illustrates another embodiment of a portion of a card read/write mechanism which receives, inserts and removes a memory card and aligns it in a particular orientation relative to a read/write assembly;

[00014] Figure 8 illustrates a control system for use with the Figure 7 embodiment;

[00015] Figure 9 shows use of the invention as part of a computer system; and

[00016] Figure 10 is a perspective view of a portion of a locking mechanism which can be used in the invention.

DETAILED DESCRIPTION OF THE INVENTION

[00017] Figure 1 shows one proposed PCRAM semiconductor memory structure which is based on a DRAM memory cell architecture. A brief description of this proposal is deemed helpful in understanding the invention. As shown in Figure 1, a memory structure 100 formed by a pair of memory cells 101 are connected to a common bit line 116 through a pair of access transistors 111. Each memory cell 101 includes a programmable conductor material layer 102, having upper 103 and lower 105 electrodes. The programmable conductor material layer has a resistance state which can change between two different values with appropriate voltage applied to the upper 103 and lower 105 electrodes. One suitable and exemplary programmable conductor material for layer 102 is a chalcogenide glass, for example a Ge:Se glass having a 20% – 30% germanium and 70% – 80% percent selenium which is doped with silver.

[00018] The lower electrodes 105 are connected to Tungsten plugs 104. The upper electrodes 103 are commonly connected to a cell plate 106. The arrangement is similar to that used in a conventional DRAM, except that the cell capacitors normally provided in a DRAM are replaced by the programmable conductor memory element 110 formed by the programmable conductor material layer 102 and the upper 103 and lower 105 electrodes. For purposes of simplifying further discussion, the programmable conductor material layer will be assumed to be a doped chalcogenide glass layer, but it should be understood that any programmable conductor material can be used.

[00019] Normally the programmable conductor glass memory element 110 is in a high resistance state, but it can be programmed to a low resistance state by

application of a suitable voltage across memory element 110. Access transistors 111 are connected to separate word lines (not shown) which are activated to couple the memory elements 110 to the bit line 116, and thereby apply suitable voltages across the memory element 110 for both programming the memory element to a low resistance state as well as erasing a memory element back to a high resistance state.

[00020] The lower resistance state of the memory element 110 occurs due to the growth of a conductive dendrite within or on the surface of the chalcogenide glass layer 102 by the voltage applied to the conductors 103, 105. This dendrite is non-volatile in that it remains when the voltage across the cell is removed.

[00021] The lower resistance state of the memory element 110 occurs due to the fact that the cell 101 has grains or quantum dots which span the upper 103 and lower 105 electrodes of the cell 101. These grains may or may not be metallic in content. When a potential is applied across the cell 101, metal ions migrate into these structures and lower the resistivity of the cell by clustering in/on the grains and ultimately connecting the grains. A reversal in the potential across the cell essentially pushes the metal ions out of these grains, thus increasing the resistance of the cell. Thus, to return the cell 101 to a high resistance state a reverse voltage at least equal to the program voltage required to program the cell 101 to a low resistant state is applied across the conductors 103, 105.

[00022] A memory element 110 is typically read by applying the voltage across it which is less than that required for writing the memory element 110 to a low resistance state. This voltage is discharged through the resistance of the

memory element 110 and the discharging voltage is read at some point to determine the high or low resistance state of the memory element and thus a stored binary value.

[00023] Although Figure 1 illustrates an exemplary architecture useful for explaining how a programmable conductor memory element 110 works, the representation shown in Figure 1 is for illustration only, as many different other arrangements for reading from and writing to a programmable conductor memory element may be employed. In addition, the particular arrangement in which the memory element 110 receives voltages from bit line 116 through access transistor 111 and cell plate 106 may also change.

[00024] The present invention utilizes the overall memory cell 101 architecture shown in Figure 1, but rearranges the programmable memory elements in a manner which provides the memory elements 110 in one or more arrays on a removable memory card 200. Thus, Figure 2 shows a programmable conductor material card 200 which is provided with an array of PCRAM memory elements 202. In an exemplary embodiment, the programmable conductor card 200 is formed of a chalcogenide glass which has between 20% - 30% germanium and between 70% - 80% selenium and is doped with silver. The card 200 may have a conductor 204 provided on one surface which may be formed of a metal such as tungsten.

[00025] The card 200 is passive in that it does not contain any access transistors, or bit lines or word lines, but only contains the programmable conductor material in which areas 202 are available for use as memory cells. It should be noted that although Figure 2 shows a regular array of memory

elements 202, the locations of memory elements 202 need not be predefined in the memory card 200, but can instead be defined by the locations on memory card 200 where conductive elements of a read/write assembly 358, described below, are located relative to the memory card 200.

[00026] Another characteristic of one embodiment of a memory card 200, shown at Figure 2B, is that the back side contains a plurality of slots 208. These slots are formed as recesses or depressions within the memory card 200 for alignment and locking purposes, as will be described below with respect to the read/write device shown in Figure 3A and Figure 3B.

[00027] In order to define the locations of the PCRAM elements 202 in the memory card 200, as well as to read from and write to those memory elements, access transistors, bit lines and word lines of a read/write assembly necessary to operate the memory elements 202 are contained within the read/write device illustrated in Figures 3A and 3B.

[00028] Figure 3A shows a device housing 302 having a front opening 303 which is designed to receive a memory card 200. Also illustrated on the front of housing 302 below the receiving slot 303 is a push button 354 for releasing a memory card 200 from the housing 302. The opening 303 may be provided with a door 319 which opens when a card is inserted into housing 302 through opening 303.

[00029] Figure 3B illustrates in side view a cross-section of the read/write mechanism contained within housing 302. The mechanism includes an upper conductive plate 306 on one side of an opening area which receives a memory card 200 which is biased by springs 354 or other biasing means towards a

read/write assembly 358 provided on an opposite side of the open area in the housing. Plate 306 has a plurality of apertures therein at a side of the housing 302 removed from opening 303. These apertures allow terminal ends of L-shaped pivot arms 340 to project through plate 306 and engage with the slots 208 on the back side of a memory card.

[00030] The pivot arms 340 shown in greater detail in Figure 10, partially project through the apertures in bias plate 306. A memory card 200 inserted into housing 302 pushes a leading edge 341 of the pivot arms 340 upward against a biasing force, for example spring 342, until the card slots 208 are aligned with the leading edge 341 of pivot arms 340, in which case the biasing on the arms 340 causes the pivot arms to move into the slots 208 and lock the memory card 200 in a held and aligned position within housing 302. When inserted into housing 302, the card 200 is also pushed against an end element 350 biased by spring 352. Thus, upon insertion of the memory card 200 into the housing 302, the end of the memory card 200 pushes against end element 350 and against bias spring 352 until the pivot arms 340 lock the memory card 200 in place.

[00031] The memory card 200 can be released by pressing on a button 354 which connects with a rod 346 having on one end an incline surface 356 against the bias of spring 348. By pushing on button 354, the incline surface 356 raises a rod 344 which pushes pivot arms 340 against the bias force, causing them to be removed from the memory card 200. When the memory card is released by the pivot arms 340, the bias on an end element 350 causes element 350 to push the memory card partially out of opening 303, where it may be grasped and removed by a user.

[00032] A read/write assembly 358 is also provided within housing 302 and is illustrated in perspective view in Figure 4. The read/write head assembly 358 includes a plurality of upwardly projecting conductive elements 304. The locations of conductive elements 304 relative to a memory card 200 inserted within the housing 302 define the location of the memory cells 202 illustrated in Figure 2A. That is, an electrical path can be established between each conductive element 304, a portion or area of the memory card 200 formed of programmable conductor material touched by the elements 304, and the common electrode 204 of the memory card, which is in turn connected to the common electrode 306 within the housing 302. The conductive elements 304 may be formed of silver when the programmable conductor material is a Ge:Se chalcogenide glass compilation doped with silver.

[00033] Figure 5 illustrates in somewhat greater detail a portion of the read/write assembly 358 for a single memory element which is formed as a semiconductor structure built over a semiconductor substrate containing a conductive well, such as a p-well. As illustrated in Figure 5, an access transistor 364, (e.g. an n-type transistor fabricator within the p-well) is provided which couples a bit line 326 through the access transistor 364 to a polysilicon plug 322 which connects to the conductive element 304.

[00034] As also illustrated in Figure 5, when the memory card 200 is provided within the housing, each conductive element 304 defines a memory element 202 with conductive element 304 functioning as the Figure 1 lower electrode 105 and the memory card conductor 204 and housing 302 conductor 306 functioning as the Figure 1 upper electrode 103. Although Figure 5 illustrates a single conductive element 304 and associated access transistor, it

should be appreciated that this structure is repeated throughout the read/write assembly 358, as shown in Figure 4 for each memory element.

[00035] Figure 6 illustrates an electrical schematic depiction of a portion of a memory array created by the contact of the read/write assembly 358 with the memory card 200. Figure 6 also illustrates bit lines, e.g. bit lines 326, 327 connected to a column decoder 380 and row lines, e.g. 362, 363, connected between a row decoder 381, and the gates of access transistors 364. When a selected row line and bit line are activated, the access transistor connected to both functions to couple an associated programmable conductor element 202 between the bit line and the common plate 306. For example, if bit line 326 and row line 362 are active an access transistor 364a connected to both couples a selected programmable bit line conductor element 202 between bit line 326 and common electrode 206, 306. Thus, by providing suitable voltages on a bit line, the common conductor 306 and a row line, a selected memory element 202 may be read, written and erased.

[00036] It should be noted that although the conductive elements 304 have been illustrated in the various figures as having a pointed or tipped configuration, they may in fact be constructed as rounded bumps or flat surfaces as well, the important point being that the conductive elements 304 provide one of the two required electrodes on opposite sides of a programmable conductor material of card 200 suitable to provide, with the common electrode 204, appropriate voltages across the programmable conductor material to define memory elements 202 which can read, written and erased.

[00037] When the memory card 200 is locked into position relative to the read/write assembly 358 alignment is achieved between the card 200 and the read/write assembly 358 so that a memory card which is programmed in one housing 302 can be removed from that housing and inserted into another like housing 302 and be properly read/written.

[00038] To further enhance the ability of the memory card 200 to be properly aligned relative to the conductive elements 304 of different read/write assemblies 358 provided in differing housings 302, it may be desirable to provide a more sophisticated control system for automatically aligning the memory card 200 with the read/write assembly 358.

[00039] Figure 7 and Figure 8 illustrate one mechanism which may be provided within housing 302 to provide an automatic insertion and removal of a memory card in the housing, as well as proper alignment of the memory card relative to the read/write assembly 358. A plurality of rollers 405 (Figure 7) may be provided on shafts which are connected to respective motors 403. When a card is inserted through opening 303 of housing 302, a card insertion switch 411 (Figure 8) is activated which provides a signal to a controller 417 which instructs the motors 403 to grab the card and drive it into the housing 302.

[00040] The controller 417 can control the motors 403 to move the card in a removal as well as insertion direction as illustrated by the arrows of Figure 7. Pushing removal button 354 in this embodiment closes a card removal switch 413, which causes controller 417 to release the card by driving the rollers 405 in a card removal direction. Controller 417 can also fine tune the location of the card 200 within the housing 302 to ensure that the card 200 is properly aligned

with respect to the conductive elements 304 of read/write assembly 358. This is done by controlling both the motors 403 which control the insertion and removal of the card, and its terminal position in the insertion/removal direction, as well as an additional motor 407 which drives a roller 409, which in turn is coupled to a frame 401 on which the motors 403 are mounted.

[00041] The frame 401 is driven by motor 407 in a lateral direction relative to the card insertion and removal direction. Thus, by appropriately controlling motor 407 as well as the motors 403, controller 417 can position an inserted card in a precise longitudinal and lateral position relative to the read/write conductors 304 of the read/write assembly 358.

[00042] In addition, as shown in Figure 8, each memory card 200 may also be provided with specific memory elements 202a arranged in a predetermined pattern which is designed to align with read/write elements 304a provided in a read/write assembly 358. The memory elements 202a, which are prerecorded with binary data, can be read when the card 200 is inserted into a housing 302, with the outputs of the memory elements 202a being provided to a decoder 419 which indicates to controller 417 when a proper alignment of the memory card 200 relative to the card read/write head assembly 358 occurs. Thus, controller 417 can appropriately drive the motors 403 and 407 until it recognizes the proper alignment pattern set by the memory elements 202a and thereby position the card 200 appropriately relative to the conductive elements 304 of the read/write assembly 358. In lieu of programmed memory elements 202a, an optically readable alignment pattern may be provided on memory card 200 which can be read by an optical reader within the housing to supply input signals

to controller 417 which are used to produce and sense proper alignment of card 200 relative to read/write assembly 358.

[00043] The controller 417 illustrated in Figure 8 is also arranged to provide an enable signal on line 480 when alignment is achieved between card 200 and read/write assembly 358. The enable signal is provided to control circuitry for the read/write assembly to enable operation of the read/write assembly 358.

[00044] An additional feature of the invention is the ability to store information in the memory card 200 as temporary or permanent data. For temporary data storage appropriate voltages are applied to bit lines, cell plate and gate of the access transistor of a memory cell. The voltage chosen will cause a memory element 202a which is in an at rest high resistance state to be programmed to a low resistance state. For example, for a chalcogenide glass composition of Ge_{25}:Se_{75} doped with silver a voltage V_1 (Figure 6) of .25v across the memory element may be used to program a memory element to the low resistance state. A negative voltage of the same or slightly higher magnitude can then be used to program a low resistance cell to a high resistance state. A voltage V_1 which is slightly less (e.g. .1v) than the voltage used to write a cell to the low resistance state can be used to read the cell.

[00045] A user has a choice of causing read/write assembly 358 to change one or more memory elements 202 from semi-volatile (re-writable) state to permanent (Read-Only Memory) state. This can be done by adjusting the write voltage upward to range between 1.5 – 3.0 volts for permanent storage, compared to the .25 volts used for semi-volatile storage. Also, some memory elements of the memory card 200 can be written permanently with the high

voltage and used as a ROM, while other memory elements 202 of the same memory card can be written as semi-volatile (re-writable) memory elements, or all memory elements of a card may be permanent storage memory elements or all memory elements may be temporary storage memory elements.

[00046] Figure 9 is a block diagram of a processor-based system 400 utilizing a removable card PCRAM array 200 constructed in accordance with the embodiments of the present invention disclosed above. The processor-based system 400 may be a computer system, a process control system or any other system employing a processor and associated memory. The system 400 includes a central processing unit (CPU) 402, e.g., a microprocessor, that communicates with the PCRAM card read/write device 302 which reads and writes to a memory card 200 and an I/O device 404 over a bus 420. It must be noted that the bus 420 may be a series of buses and bridges commonly used in a processor-based system, but for convenience purposes only, the bus 420 has been illustrated as a single bus. A second I/O device 406 is illustrated, but is not necessary to practice the invention. The processor-based system 400 also includes read-only memory (ROM) 410 and may include peripheral devices such as a floppy disk drive 412 and a compact disk (CD) ROM drive 414 that also communicates with the CPU 402 over the bus 420 as is well known in the art.

[00047] While the invention has been described and illustrated with reference to specific exemplary embodiments, it should be understood that many modifications and substitutions can be made without departing from the spirit and scope of the invention. Accordingly, the invention is not to be considered as limited by the foregoing description but is only limited by the scope of the appended claims.